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DESIGN OF 4x4 BIT SRAM USING VHDL

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ABSTRACT

Memory arrays are an essential building block in any digital system. The aspects of designing an SRAM are very vital to designing other digital circuits as well. The majority of space taken in an integrated circuit is the memory. SRAM design consists of key considerations, such as increased speed and reduced layout area. The hope for this project was to be able to create an efficient and compact SRAM. Due to time limitations, the goal was to create a working SRAM design and to learn how the SRAM functions. Design choices were made and justified appropriately. RAM has become a major component in many VLSI Chips due to their large storage density and small access time. SRAM has become the topic of substantial research due to the rapid development for low power, low voltage memory design during recent years due to increase demand for notebooks, laptops, IC memory cards and hand held communication devices. SRAMs are widely used for mobile applications as both on chip and off chip memories, because of their ease of use and low standby leakage .The main objective of this paper is evaluating performance in terms of Power consumption, delay .

Keywords— SRAM, VLSI, Read-Static Noise Margin (SNM), Stability and Power Consumption, SPLD, CPLD, FPGA.

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Chapter 1

INTRODUCTION TO MEMORY UNIT

1.1 OVERVIEW

A Memory unit is a device to which binary information is transferred for storage and from which information is available when needed for processing. When data processing takes place, information from the memory is transferred to selected registers in the processing unit. Inter- mediate and final results obtained in the processing unit are transferred back to be stored in memory. A memory unit is a collection of cells capable of storing a large quantity of binary information.

There are three types of memories that are used in digital systems: RANDOM – ACCESS MEMORY(RAM) and READ-ONLY MEMORY(RAM) or a Hybrid of two . RAM accepts new information for storage to be available later for use. The process of storing new information into memory is referred to as a memory write operation. The process of transferring the stored information out of memory is referred to as a memory read operation. RAM can perform both the read and write operations. ROM can perform only the read operation. This means that a suitable binary information is already stored inside the memory, which can be read or retrieved at any time.

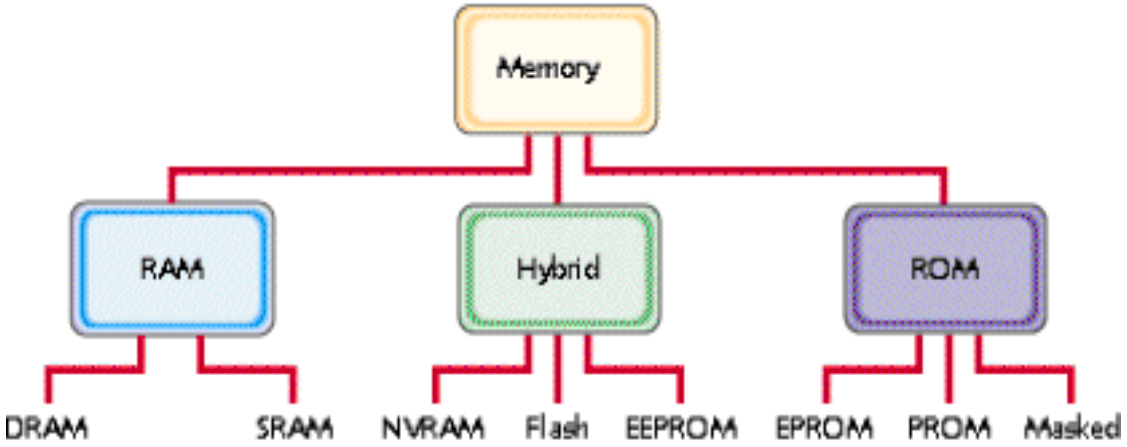

Figure 1 : Common memory types in embedded systems

The RAM family includes two important memory devices: static RAM (SRAM) and dynamic RAM (DRAM). The primary difference between them is the lifetime of the data they store. SRAM retains its contents as long as electrical power is applied to the chip. If the power is turned off or lost temporarily, its contents will be lost forever. DRAM, on the other hand, has an extremely short data lifetime-typically about four milliseconds. This is true even when power is applied constantly.

In short, SRAM has all the properties of the memory you think of when you hear the word RAM. Compared to that, DRAM seems kind of useless. By itself, it is. However, a simple piece of hardware

called a DRAM controller can be used to make DRAM behave more like SRAM. The job of the DRAM controller is to periodically refresh the data stored in the DRAM. By refreshing the data before it expires, the contents of memory can be kept alive for as long as they are needed. So DRAM is as useful as SRAM after all.

When deciding which type of RAM to use, a system designer must consider access time and cost. SRAM devices offer extremely fast access times (approximately four times faster than DRAM) but are much more expensive to produce. Generally, SRAM is used only where access speed is extremely important. A lower cost-per-byte makes DRAM attractive whenever large amounts of RAM are required. Many embedded systems include both types: a small block of SRAM (a few kilobytes) along a critical data path and a much larger block of DRAM (perhaps even Megabytes) for everything else.

Type	*Volatile ?*	*Writeable?*	*Erase Size*	*Max Erase Cycles*	*Cost (per Byte)*	*Speed*
SRAM	Yes	Yes	Byte	Unlimited	Expensive	Fast
DRAM	Yes	Yes	Byte	Unlimited	Moderate	Moderate
Masked ROM	No	No	n/a	n/a	Inexpensive	Fast
PROM	No	Once, with a device programmer	n/a	n/a	Moderate	Fast
EPROM	No	Yes, with a device programmer	Entire Chip	Limited (consult datasheet)	Moderate	Fast
EEPROM	No	Yes	Byte	Limited (consult datasheet)	Expensive	Fast to read, slow to erase/write
Flash	No	Yes	Sector	Limited (consult datasheet)	Moderate	Fast to read, slow to erase/write
NVRAM	No	Yes	Byte	Unlimited	Expensive (SRAM + battery)	Fast

Table 1 : Characteristics of the various memory types

1.2 AIM OF THE PROJECT

The main purpose of the project is to design and develop the 4*4 bit Static Random Access Memory.

A typical VLSI or embedded system designing can be divided into two sections , the Front-end and the Back-end. The back-end typically consists of the process related to the fabrication of the design on actual silicon or germanium or any such suitable semiconductor elements. The other part is called the